

74HC164; 74HCT164

8-bit serial-in, parallel-out shift register

Product data sheet

1. General description

The 74HC164; 74HCT164 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC164; 74HCT164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q0, which is the logical AND of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset ($\overline{\text{MR}}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

2. Features

- Gated serial data inputs
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

3. Quick reference data

Table 1: Quick reference data
 $GND = 0\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC164						
t_{PHL} , t_{PLH}	propagation delay					
	CP to Qn	$C_L = 15\text{ pF}$; $V_{\text{CC}} = 5\text{ V}$	-	12	-	ns
	$\overline{\text{MR}}$ to Qn	$C_L = 15\text{ pF}$; $V_{\text{CC}} = 5\text{ V}$	-	11	-	ns

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Table 1: Quick reference data ...continued

$GND = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $t_r = t_f = 6\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum clock frequency	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	78	-	MHz
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per package		[1] [2]	40	-	pF
Type 74HCT164						
t_{PHL}, t_{PLH}	propagation delay					
	CP to Qn	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	14	-	ns
	\overline{MR} to Qn	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	16	-	ns
f_{max}	maximum clock frequency	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	61	-	MHz
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per package		[1] [3]	40	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

N = number of inputs switching

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

[2] For HC the condition is $V_I = GND$ to V_{CC} .

[3] For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5\text{ V}$.

4. Ordering information

Table 2: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC164N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC164D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm	SOT108-2
74HC164DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC164PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT164N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT164D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm	SOT108-2

Table 3: Pin description ...continued

Symbol	Pin	Description
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH, edge-triggered)
$\overline{\text{MR}}$	9	master reset input (active LOW)
Q4	10	output
Q5	11	output
Q6	12	output
Q7	13	output
V _{CC}	14	positive supply voltage

7. Functional description

7.1 Function selection

Table 4: Function table [1]

Operating modes	Input				Output	
	$\overline{\text{MR}}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

[1] H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input diode current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output diode current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output source or sink current	V _O = -0.5 V to V _{CC} + 0.5 V	-	±25	mA
I _{CC} , I _{GND}	V _{CC} or GND current		-	±50	mA
T _{stg}	storage temperature		-65	+150	°C

Table 5: Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation				
	DIP14 package		[1] -	750	mW
	SO14; SSOP14; TSSOP14; DHVQFN14 package		[2] -	500	mW

[1] For DIP14 packages: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO14 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.

For SSOP14 and TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC164						
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
t _r , t _f	input rise and fall time	V _{CC} = 2.0 V	-	-	1000	ns
		V _{CC} = 4.5 V	-	6.0	500	ns
		V _{CC} = 6.0 V	-	-	400	ns
T _{amb}	ambient temperature		-40	-	+125	°C
Type 74HCT164						
V _{CC}	supply voltage		4.5	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
t _r , t _f	input rise and fall time	V _{CC} = 4.5 V	-	6.0	500	ns
T _{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics for 74HC164

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V

Table 7: Static characteristics for 74HC164 ...continued
 At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	μA
C _I	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.84	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.34	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.33	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	μA

Table 7: Static characteristics for 74HC164 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}		-		
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}		-		
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	160	μA

Table 8: Static characteristics for 74HCT164

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 2.1 V; other inputs V _I = V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A	-	100	360	μA
C _I	input capacitance		-	3.5	-	pF

11. Dynamic characteristics

Table 9: Dynamic characteristics for 74HC164

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; test circuit see [Figure 10](#); unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$T_{\text{amb}} = 25\text{ °C}$							
$t_{\text{PHL}}, t_{\text{PLH}}$	propagation delay CP to Qn	see Figure 7					
		$V_{\text{CC}} = 2.0\text{ V}$	-	41	170	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	15	34	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	12	29	ns	
t_{PHL}	propagation delay MR to Qn	see Figure 8					
		$V_{\text{CC}} = 2.0\text{ V}$	-	39	140	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	14	28	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	11	24	ns	
$t_{\text{THL}}, t_{\text{TLH}}$	output transition time	see Figure 7					
		$V_{\text{CC}} = 2.0\text{ V}$	-	19	75	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	7	15	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	6	13	ns	
t_w	clock pulse width; HIGH or LOW	see Figure 7					
		$V_{\text{CC}} = 2.0\text{ V}$	80	14	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	16	5	-	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	14	4	-	ns	
	master reset pulse width; LOW	see Figure 8					
		$V_{\text{CC}} = 2.0\text{ V}$	60	17	-	ns	
$V_{\text{CC}} = 4.5\text{ V}$		12	6	-	ns		
	$V_{\text{CC}} = 6.0\text{ V}$	10	5	-	ns		
t_{rem}	removal time $\overline{\text{MR}}$ to CP	see Figure 8					
		$V_{\text{CC}} = 2.0\text{ V}$	60	17	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	12	6	-	ns	
	$V_{\text{CC}} = 6.0\text{ V}$	10	5	-	ns		
t_{su}	set-up time DSA, and DSB to CP	see Figure 9					
		$V_{\text{CC}} = 2.0\text{ V}$	60	8	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	12	3	-	ns	
	$V_{\text{CC}} = 6.0\text{ V}$	10	2	-	ns		
t_h	hold time DSA and DSB to CP	see Figure 9					
		$V_{\text{CC}} = 2.0\text{ V}$	+4	-6	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	+4	-2	-	ns	
	$V_{\text{CC}} = 6.0\text{ V}$	+4	-2	-	ns		
f_{max}	maximum clock pulse frequency	see Figure 7					
		$V_{\text{CC}} = 2.0\text{ V}$	6	23	-	MHz	
		$V_{\text{CC}} = 4.5\text{ V}$	30	71	-	MHz	
	$V_{\text{CC}} = 6.0\text{ V}$	35	85	-	MHz		

Table 9: Dynamic characteristics for 74HC164 ...continued

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; test circuit see [Figure 10](#); unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$T_{amb} = -40\text{ °C to }+85\text{ °C}$							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7					
		$V_{CC} = 2.0\text{ V}$	-	-	215	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	43	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	37	ns	
t_{PHL}	propagation delay MR to Qn	see Figure 8					
		$V_{CC} = 2.0\text{ V}$	-	-	175	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	35	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	30	ns	
t_{THL}, t_{TLH}	output transition time	see Figure 7					
		$V_{CC} = 2.0\text{ V}$	-	-	95	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	19	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	16	ns	
t_w	clock pulse width; HIGH or LOW	see Figure 7					
		$V_{CC} = 2.0\text{ V}$	100	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	20	-	-	ns	
		$V_{CC} = 6.0\text{ V}$	17	-	-	ns	
	master reset pulse width; LOW	see Figure 8					
		$V_{CC} = 2.0\text{ V}$	75	-	-	ns	
$V_{CC} = 4.5\text{ V}$		15	-	-	ns		
	$V_{CC} = 6.0\text{ V}$	13	-	-	ns		
t_{rem}	removal time \overline{MR} to CP	see Figure 8					
		$V_{CC} = 2.0\text{ V}$	75	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	15	-	-	ns	
	$V_{CC} = 6.0\text{ V}$	13	-	-	ns		
t_{su}	set-up time DSA and DSB to CP	see Figure 9					
		$V_{CC} = 2.0\text{ V}$	75	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	15	-	-	ns	
	$V_{CC} = 6.0\text{ V}$	13	-	-	ns		
t_h	hold time DSA and DSB to CP	see Figure 9					
		$V_{CC} = 2.0\text{ V}$	4	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	4	-	-	ns	
	$V_{CC} = 6.0\text{ V}$	4	-	-	ns		
f_{max}	maximum clock pulse frequency	see Figure 7					
		$V_{CC} = 2.0\text{ V}$	5	-	-	MHz	
		$V_{CC} = 4.5\text{ V}$	24	-	-	MHz	
	$V_{CC} = 6.0\text{ V}$	28	-	-	MHz		

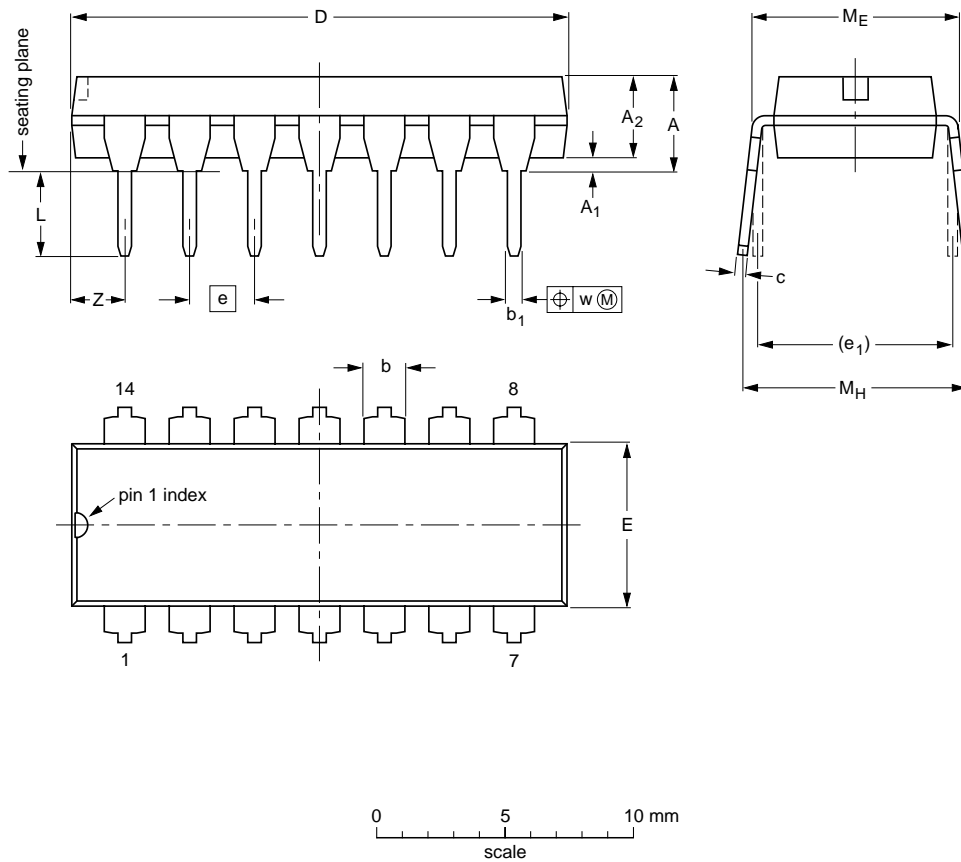
Table 9: Dynamic characteristics for 74HC164 ...continued*GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; test circuit see [Figure 10](#); unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$T_{amb} = -40$ °C to $+125$ °C							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7					
		$V_{CC} = 2.0$ V	-	-	255	ns	
		$V_{CC} = 4.5$ V	-	-	51	ns	
		$V_{CC} = 6.0$ V	-	-	43	ns	
t_{PHL}	propagation delay MR to Qn	see Figure 7					
		$V_{CC} = 2.0$ V	-	-	210	ns	
		$V_{CC} = 4.5$ V	-	-	42	ns	
		$V_{CC} = 6.0$ V	-	-	36	ns	
t_{THL}, t_{TLH}	output transition time	see Figure 7					
		$V_{CC} = 2.0$ V	-	-	110	ns	
		$V_{CC} = 4.5$ V	-	-	22	ns	
		$V_{CC} = 6.0$ V	-	-	19	ns	
t_w	clock pulse width; HIGH or LOW	see Figure 7					
		$V_{CC} = 2.0$ V	120	-	-	ns	
		$V_{CC} = 4.5$ V	24	-	-	ns	
		$V_{CC} = 6.0$ V	20	-	-	ns	
	master reset pulse width; LOW	see Figure 7					
		$V_{CC} = 2.0$ V	90	-	-	ns	
$V_{CC} = 4.5$ V		18	-	-	ns		
	$V_{CC} = 6.0$ V	15	-	-	ns		
t_{rem}	removal time \overline{MR} to CP	see Figure 8					
		$V_{CC} = 2.0$ V	90	-	-	ns	
		$V_{CC} = 4.5$ V	18	-	-	ns	
	$V_{CC} = 6.0$ V	15	-	-	ns		
t_{su}	set-up time DSA and DSB to CP	see Figure 9					
		$V_{CC} = 2.0$ V	90	-	-	ns	
		$V_{CC} = 4.5$ V	18	-	-	ns	
	$V_{CC} = 6.0$ V	15	-	-	ns		
t_h	hold time DSA and DSB to CP	see Figure 9					
		$V_{CC} = 2.0$ V	4	-	-	ns	
		$V_{CC} = 4.5$ V	4	-	-	ns	
	$V_{CC} = 6.0$ V	4	-	-	ns		
f_{max}	maximum clock pulse frequency	see Figure 7					
		$V_{CC} = 2.0$ V	4	-	-	MHz	
		$V_{CC} = 4.5$ V	20	-	-	MHz	
	$V_{CC} = 6.0$ V	24	-	-	MHz		

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

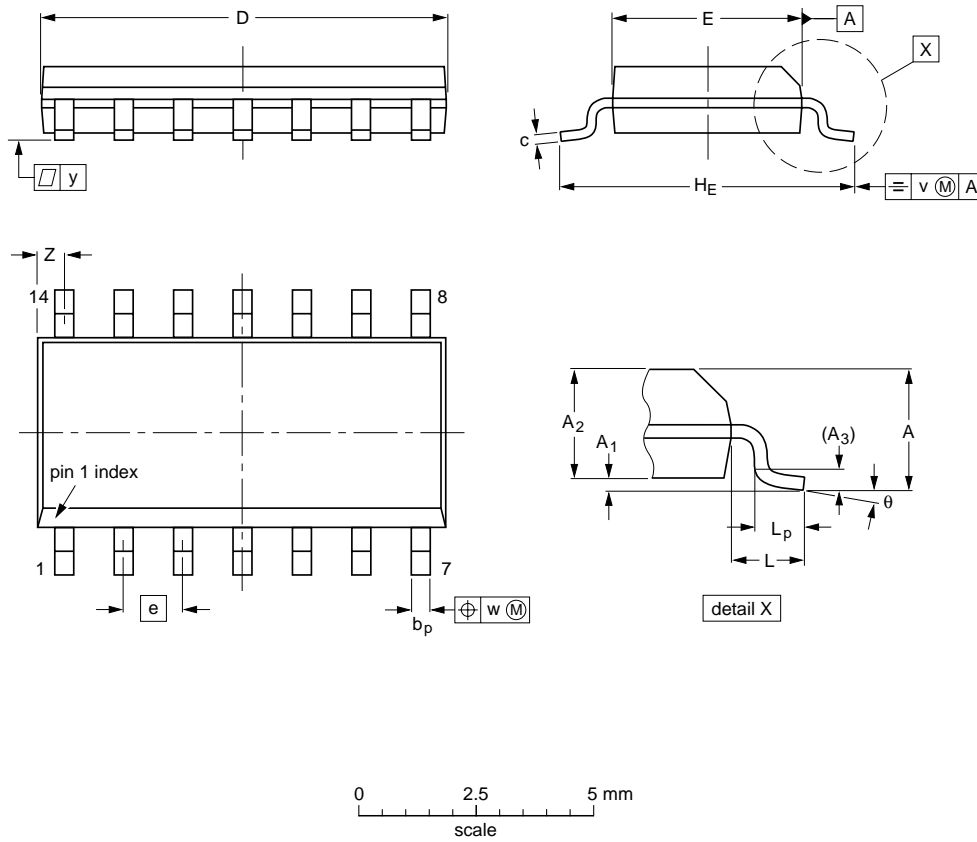
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT27-1	050G04	MO-001	SC-501-14	

Fig 11. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm

SOT108-2



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.55 1.40	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.061 0.055	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT108-2		MS-012		

Fig 12. Package outline SOT108-2 (SO14)